Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Low-Power 4-Transistor Hybrid CMOS XOR Gate

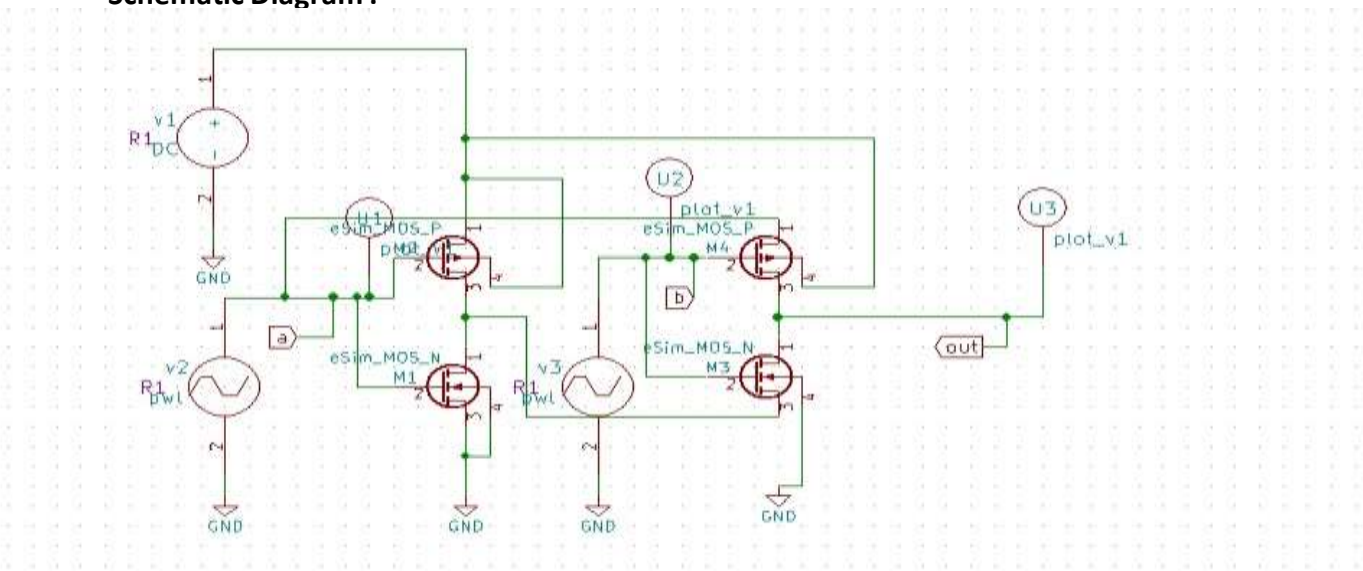
Theory/Description : The Exclusive-OR (XOR) gate is a fundamental digital logic circuit widely used in arithmetic operations, error detection, and data processing systems. The XOR function produces a logic high output when the input bits are different and a logic low when they are the same. Conventional CMOS XOR designs typically require 8 to 12 transistors, resulting in higher power consumption and larger area. In this work, a 4-transistor XOR gate is implemented using hybrid CMOS logic to achieve reduced transistor count and improved efficiency. The circuit combines a CMOS inverter stage with transistor-based switching logic to generate the XOR function. The inverter provides signal restoration, while the remaining transistors control the output based on input combinations. Due to this combination of CMOS and switching logic, the circuit is classified as a hybrid CMOS design. This approach reduces hardware complexity and power consumption, though it may introduce slight voltage degradation due to threshold voltage effects.

Reason to reproduce with eSim : This circuit is ideal for simulation in eSim as it demonstrates transistor-level optimization and hybrid CMOS logic design techniques. Using eSim (Ngspice), the circuit can be simulated to verify XOR functionality, analyze power consumption, and observe propagation delay. The platform also enables waveform visualization, helping to study switching behavior and voltage characteristics. This makes the design suitable for both academic learning and research-oriented analysis in low-power VLSI design.

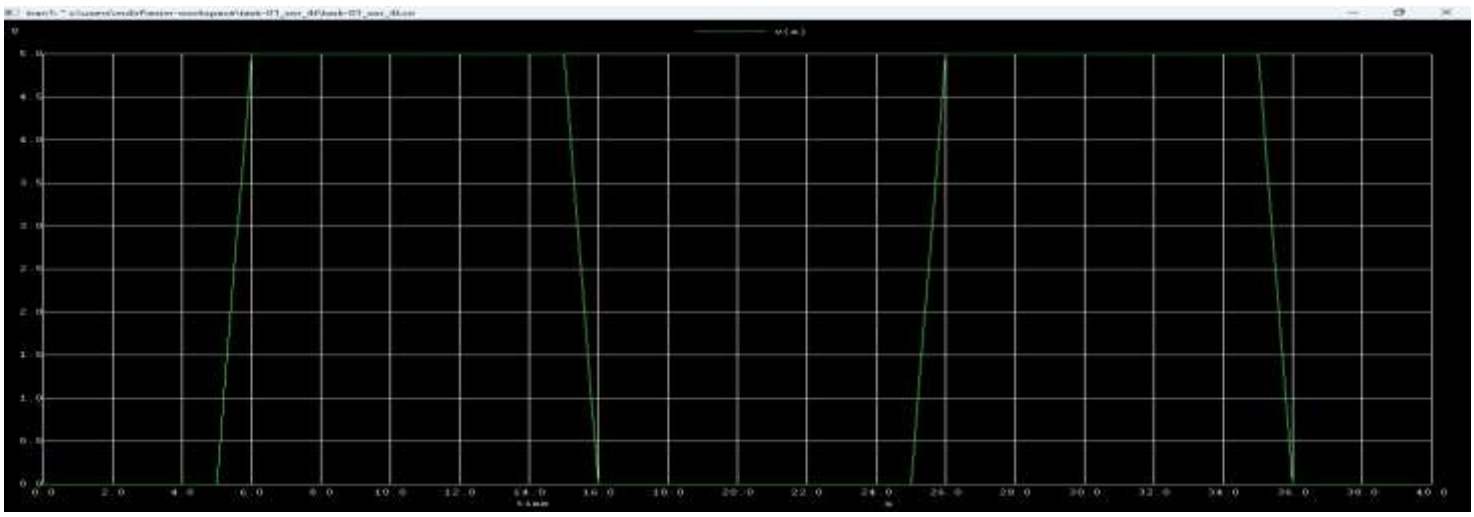
Expected Outcome/outputs : The circuit will correctly implement XOR logic, where the output is high when the inputs are different and low when they are the same. Simulation results will show proper output waveforms corresponding to all input combinations. The design is expected to use fewer transistors compared to conventional CMOS XOR circuits, resulting in improved power efficiency and compact implementation. Minor voltage degradation may be observed due to the reduced transistor configuration, but overall functionality will remain correct.

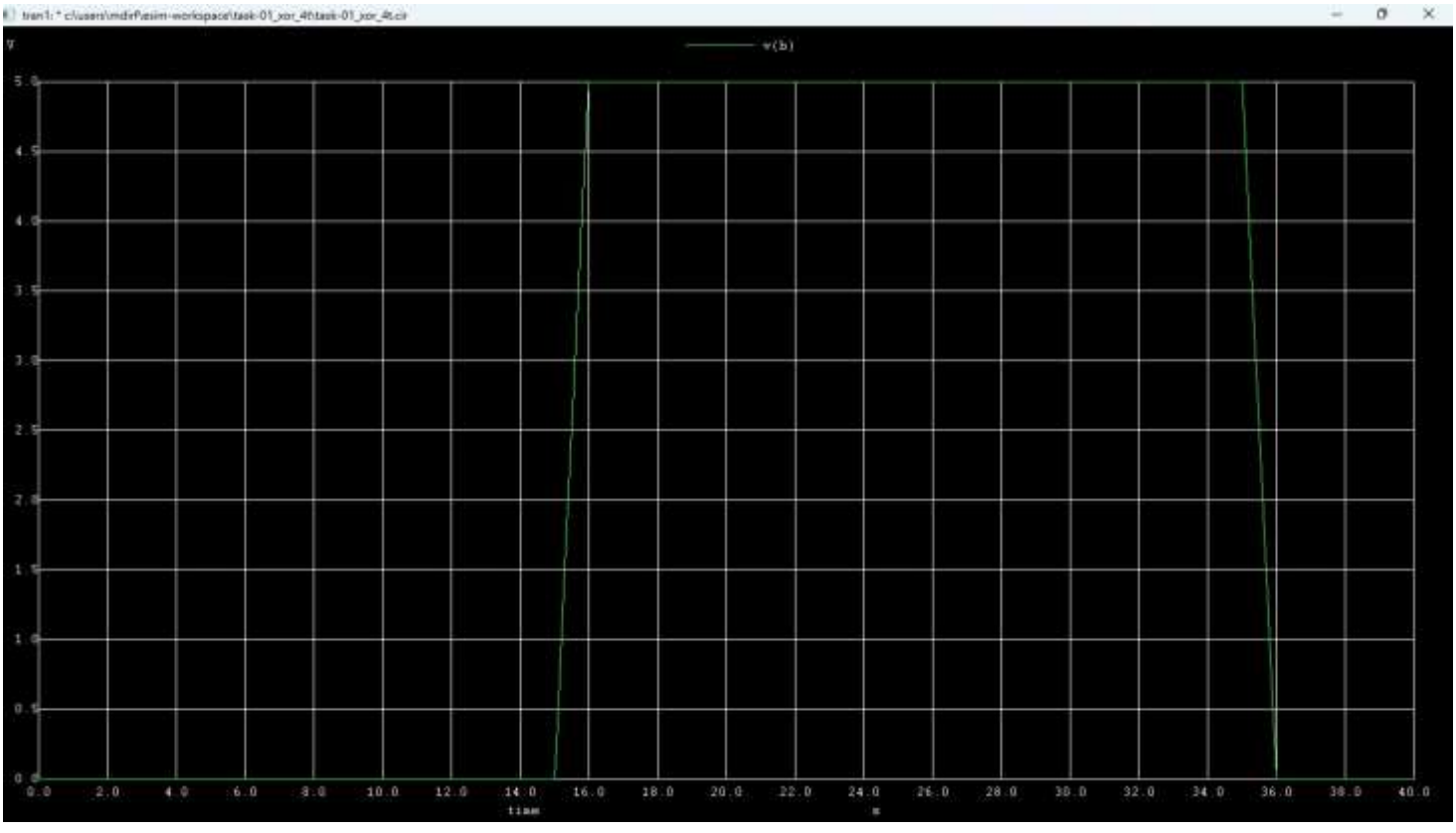
Circuit Diagram(s) :Full schematic showing two input lines (A and B), CMOS inverter stage, switching transistors, output node (Y), and connections to power supply (VDD) and ground (GND).
Components: PMOS transistors, NMOS transistors, DC voltage source (VDD), pulse voltage sources for inputs (A and B), ground, and connecting wires.

Schematic Diagram :

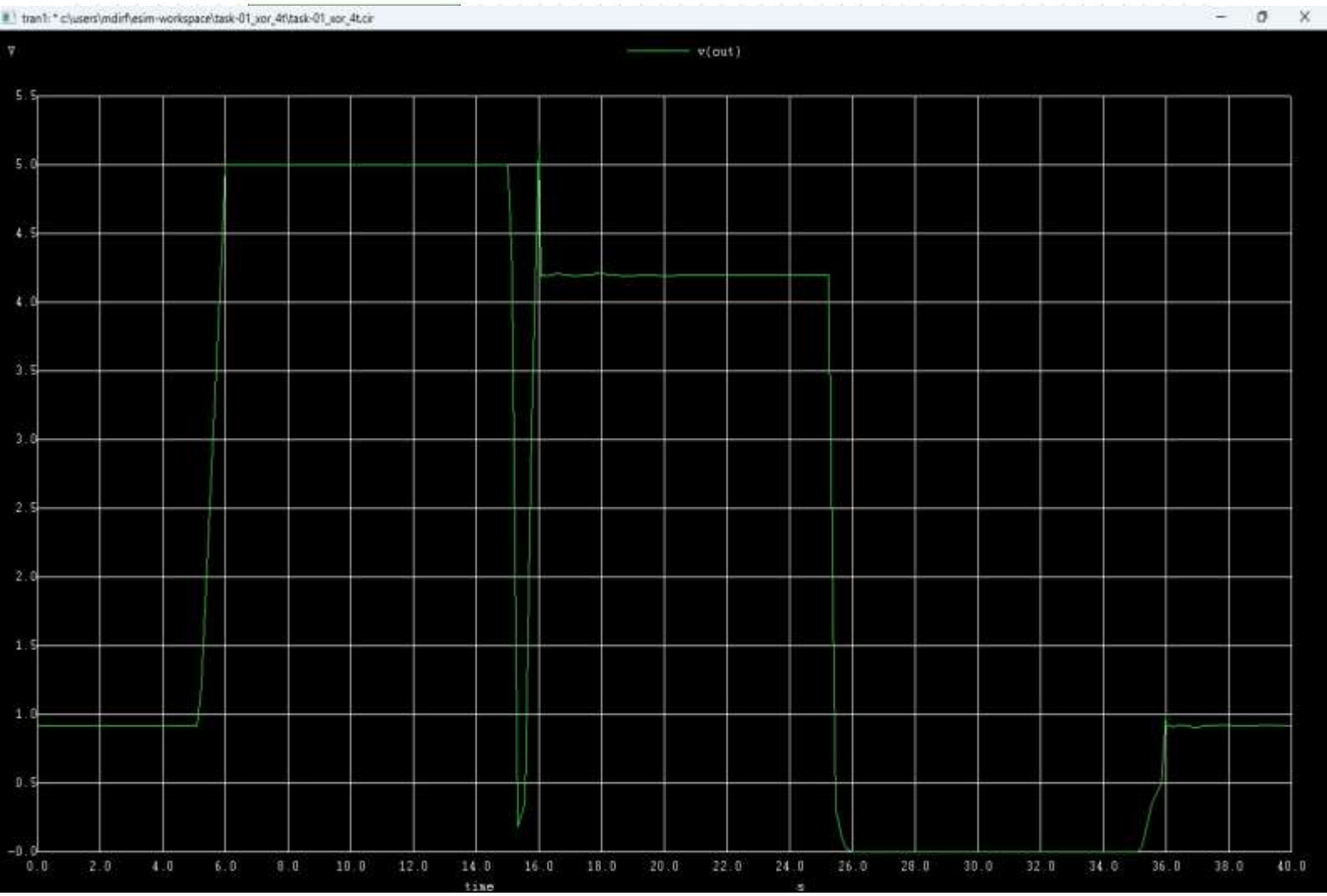


Simulation Output :





Simulation Output:



Block Diagram (s) :

Single block showing:

- Inputs: Two input signals (A, B)
- Processing Block: Hybrid CMOS XOR logic (inverter + switching transistors)
- Output: XOR output (Y)

Expected Results (Input, Output waveforms and/or Multimeter readings) :

- Input: Two digital input signals (A and B) with all possible combinations (00, 01, 10, 11)
- Output: Corresponding XOR output where Y = 1 for inputs 01 and 10, and Y = 0 for inputs 00 and 11.
  The simulation in eSim will produce correct output waveforms showing proper transitions based on input changes. The output waveform will reflect XOR functionality with minimal delay.

- Slight reduction in voltage levels may be observed due to reduced transistor count, but the logical operation will remain correct.

Research Paper/Journal/etc. :

- **Title:** "Performance Analysis of Low Power XOR-XNOR Circuits for VLSI Applications"
- **Author:** Subodh Wariya, Rajendra Kumar Nagaria and Sudarshan Tiwari
- **Page No.:** 4
- **Link:**https://www.researchgate.net/publication/228534271_Performance_Analysis_of_High_Speed_Hybrid_CMOS_Full_Adder_Circuits_for_Low_Voltage_VLSI_Design

Source/Reference(s) :

- Weste, Neil H. E., and David Harris. *CMOS VLSI Design: A Circuits and Systems Perspective.* Pearson**.**
- Rabaey, Jan M. *Digital Integrated Circuits: A Design Perspective.* Pearson
- **Wikipedia:** XOR Gate. https://en.wikipedia.org/wiki/XOR_gate
- **eSim Documentation: https://esim.fossee.in/resources**
